CLAIMS

What is claimed is:

1. A method for controlling reassembly and transmission of a packet in a communication switch, comprising:

receiving a first cell of a packet corresponding to a selected source of a plurality of sources;

allocating a reassembly context to the selected source;

storing the first cell in a buffer;

updating the reassembly context to reflect storage of the first cell in the buffer;

receiving subsequent cells of the packet;

storing each of the subsequent cells in the buffer;

updating the reassembly context as each subsequent cell is stored in the buffer; and

when a subsequent cell of the packet is determined to be an end of message cell indicating the end of the packet:

completing reassembly of the packet in the buffer to produce a reassembled packet;

queuing the reassembled packet for transmission to a destination of a

plurality destinations; and

deallocating the reassembly context.

2. The method of claim 1, wherein the reassembly context includes a head pointer and a tail pointer corresponding to the packet as stored in the buffer, wherein the packet is stored as a linked list in the buffer.

3. The method of claim 2, wherein storing each of the subsequent cells in the buffer further comprises appending each of the subsequent cells to the linked list, wherein updating the reassembly context further comprises updating the tail pointer of the linked list to reflect addition of each of the subsequent cells to the linked list.

4. The method of claim 1, wherein allocating the reassembly context further comprises allocating the reassembly context from a set of reassembly contexts.

5. The method of claim 4, wherein a number of reassembly contexts in the set of reassembly contexts is fewer than a number of sources of the plurality of sources.

6. The method of claim 1, wherein queuing the reassembled packet further comprises passing at least one control cell to a traffic management device that controls transmission of packets to at least a portion of the plurality of destinations.

7. The method of claim 1, wherein queuing the reassembled packet further comprises queuing the reassembled packet for transmission to multiple destinations of the plurality of destinations.

8. The method of claim 1, wherein queuing the reassembled packet further comprises changing encapsulation of the reassembled packet.

9. An egress circuit for a communication switch, comprising:

a context table that stores a plurality of reassembly contexts;

a buffer;

a traffic management block operably coupled to the context table and the buffer, wherein the traffic management block receives indications that packets corresponding to reassembly contexts of the plurality of reassembly contexts are ready for transmission, wherein the traffic management block transmits packets ready for transmission over at least one egress connection; and

routing circuitry operably coupled to the context table, the traffic management block, and the buffer, wherein the routing circuitry is operably coupled to receive cells corresponding to a source, wherein for a first cell received for a packet from the source, the routing circuitry allocates a first reassembly context to the source and stores the first cell in the buffer and updates the first reassembly context to reflect the storage of the first cell, wherein for subsequent cells of the packet, the routing circuitry stores the subsequent cells in the buffer and updates the first reassembly context to reflect storage of the subsequent cells, wherein when a final cell for the packet is received, the routing circuitry:

stores the final cell in the buffer;

updates the first reassembly context to reflect storage of the final cell;

provides an indication to the traffic management block that the packet corresponding to the first reassembly context is ready for transmission; and

deallocates the first reassembly context.

10. The egress circuit of claim 9, wherein the egress circuit is included in a

communications switch that includes a plurality of ingress circuits and a switching fabric, wherein the source is an ingress connection provided to one of the ingress circuits, wherein the routing circuitry receives cells corresponding to a plurality of ingress connections provided to at least a portion of the plurality of ingress circuits, wherein the routing circuitry allocates and deallocates reassembly contexts to packets received via the plurality of ingress connections.

11. The egress circuit of claim 10, wherein a number of reassembly contexts in the plurality of reassembly contexts is less than a number of ingress connections in the plurality of ingress connections.

12. The egress circuit of claim 10, wherein the communication switch is an asynchronous transfer mode switch.

13. The egress circuit of claim 9, wherein cells received for the packet are stored in the buffer as a linked list, and wherein the first reassembly context stores a head pointer and a tail pointer corresponding to the linked list.

14. The egress circuit of claim 9, wherein the traffic management block includes a plurality of queues, wherein the traffic management block queues packets awaiting transmission in one of the plurality of queues prior to transmission.

15. The egress circuit of claim 9, wherein the routing circuitry provides the indication to the traffic management block that the packet corresponding to the first reassembly context is ready for transmission by providing a control cell to the traffic management block.

16. The egress circuit of claim 15, wherein the routing circuitry provides multiple control cells to the traffic management block for the packet such that the traffic

management block transmits the packet over multiple egress connections.

17. The egress circuit of claim 16, wherein the routing circuitry provides the traffic management block with encapsulation modification information, wherein the traffic management block modifies encapsulation of the packet prior to transmission on at least one of the multiple egress connections.

18. A packet reassembly processor, comprising:

a processing module; and

memory operably coupled to the processing module, wherein the memory stores operating instructions that, when executed by the processing module, cause the processing module to perform functions that include:

in response to receipt of a first cell of a packet corresponding to a selected source of a plurality of sources, allocating a reassembly context to the selected source;

storing the first cell in a buffer;

updating the reassembly context to reflect storage of the first cell in the buffer;

receiving subsequent cells of the packet;

storing each of the subsequent cells in the buffer;

updating the reassembly context as each subsequent cell is stored in the buffer; and

when a subsequent cell of the packet is determined to be an end of message cell indicating the end of the packet:

completing reassembly of the packet in the buffer to produce a reassembled packet;

queuing the reassembled packet for transmission to a destination of a plurality destinations; and

deallocating the reassembly context.

19. The packet reassembly processor of claim 18, wherein the reassembly context includes a head pointer and a tail pointer corresponding to the packet as stored in the buffer, wherein the packet is stored as a linked list in the buffer.

20. The packet reassembly processor of claim 19, wherein the memory includes operating instructions such that the processing module stores each of the subsequent cells in the buffer by appending each of the subsequent cells to the linked list, and wherein the instructions cause the processing module to update the reassembly context by updating the tail pointer of the linked list to reflect addition of each of the subsequent cells to the linked list.

21. The packet reassembly processor of claim 18, wherein the memory includes operating instructions such that the processing module allocates the reassembly context from a set of reassembly contexts.

22. The packet reassembly processor of claim 21, wherein a number of reassembly contexts in the set of reassembly contexts is fewer than a number of sources of the plurality of sources.

23. The packet reassembly processor of claim 21, wherein the memory includes operating instructions such that the processing module queues the reassembled packet in a manner that includes passing at least one control cell to a traffic management device that controls transmission of packets to at least a portion of the plurality of destinations.

24. The packet reassembly processor of claim 21, wherein the memory includes operating instructions such that the processing module wherein queues the reassembled packet for transmission to multiple destinations of the plurality of destinations.

25. The packet reassembly processor of claim 21, wherein the memory includes operating instructions such that when the processing module queues the reassembled packet, the processing module causes encapsulation of the reassembled packet to be changed.

26. An egress circuit for a communication switch, comprising:

routing circuitry operably coupled to receive cells corresponding to a plurality of sources, wherein for a first cell received for a packet from a particular source of the plurality of sources, the routing circuitry assigns allocates a reassembly context to the packet and outputs the cell with an indication as to the reassembly context allocated, wherein for subsequent cells received for the packet, the routing circuitry determines that the subsequent cells correspond to the packet and outputs the subsequent cells with the indication of the reassembly context, wherein for a final cell received for the packet, the routing circuitry determines that the final cell corresponds to the packet and outputs the final cell with the indication as to the reassembly context and an indication corresponding to at least one destination;

a buffer; and

a traffic management block operably coupled to the buffer and the routing circuitry, wherein the traffic management block receives cells from the routing circuitry with accompanying indications, wherein the traffic management block maintains a plurality of reassembly contexts for reassembling packets in the buffer, wherein the traffic management block stores received cells in the buffer at locations corresponding to the plurality of contexts, wherein when a final cell for a completed packet is received, the traffic management block queues the completed packet for transmission over the at least one egress connection included with the final cell for the completed packet as received from the routing circuitry, wherein the traffic management block.

27. The egress circuit of claim 26, wherein the routing circuitry performs cyclical redundancy check verification for packets received, wherein when cyclical redundancy check verification indicates that an at least partially received packet has been corrupted, the routing circuitry may cause the at least partially received packet to be purged.

28. The egress circuit of claim 26, wherein the routing circuitry deallocates reassembly contexts corresponding to packets when final cells for the packets are received.